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Transmitter and Receiver Design at L-band and X-band for FM-CW Radar Altimeter

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***Abstract*—**In recent years, there has been a growing interest in FM-CW (frequency modulated continuous wave) technology for military and civilian applications. FM-CW radar altimeters find applications to detect ground proximity during automatic landing in low-visibility condition, collision avoidance systems in vehicles, and ground penetrating radars for buried object detections such as landmines, pipelines, etc. The development of a low-power L-band and X-band FM-CW radar hardware and design of a third order loop filter for the phase locked loop (PLL) are the main focus of this paper. We provide detailed circuit description of PLL-VCO and third order loop filter for direct digital synthesis (DDS) based FM-CW generation. Results of laboratory trial for the calibration of FMCW radar hardware are presented to demonstrate the feasibility of operation at X band. All test results on actual radar hardware at X-band are described in the paper.

***Keywords*—**FMCW, DDS, PLL-VCO, phase noise, loop filter.

I. Introduction

CONTINUOUS wave radars with frequency modulated (FM-CW) modeof operation are increasingly becoming popular. The advantages of FM-CW radars are light weight, low power and cost effective design. They are widely being used in various applications like sensors in vehicle parking systems for adaptive cruise control (ACC) [1], collision avoidance in vehicles, as altimeters in safe landing of aircrafts [2], surface and ground penetrating radars to measure ice thickness and buried objects [3], etc. Continuous wave transmission allows accurate relative height measurement with low power operation.

The design consideration for FM-CW systems is a linear frequency modulation technique that determines the quality of the received beat frequency IF signal. For generating a linear analog sweep in frequency, generally a voltage controlled oscillator (VCO) is used, which is a nonlinear active device. Although the VCO-based design has the advantage of producing wide bandwidth FM sweep generation at high frequency, the nonlinearities in the frequency sweep are very prominent. A direct digital synthesizer (DDS)-based FM sweep generation system provides a comparatively lower phase noise and precise, stable linear frequency modulation.

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This paper describes a DDS-phase locked loop (PLL) combination of an L-band transmit-receive radar system, whose VCO nonlinearities are controlled by a DDS-generated reference signal to make up for a wide band operation and linear frequency modulation. A study of wideband transmitter-receiver design with PLL-VCO combination for X- and L-band radars is presented in the paper. The contribution in the design is devising a stable third order loop filter PLL for fast locking and settling time. All simulations are done in Matlab®Simulink® environment, and test results of designed hardware for transmit-receive system in case of X-band are described and discussed in this paper.

II. Background Principle of FMCW Radar Altimeter

The typical waveform modulations used in FMCW radar altimeter are sinusoidal, triangular, and saw-tooth wave. In our case, we use a saw tooth modulation as it can detect and distinguish multiple targets [4]. The frequency of the transmit signal increases linearly with time as shown in **Figure 1** and is mathematically expressed in the time-domain [5] as

$$S_t(t) = \cos 2\pi \left(f_o t + \frac{1}{2}\alpha t^2 \right) \tag{1}$$

where, f_o is the FM sweep start frequency which is the carrier frequency, $t$is the instantaneous FM sweep time variable, and $\alpha = \frac{BW}{T}$ is the FM chirp rate. BW is the FM chirp bandwidth and T is the sweep time. The received signal is a delayed version of the transmitted signal and is represented as

$$S_r(t) = \cos 2\pi (f_o(t - \tau_o) + \frac{1}{2}\alpha(t - \tau_o)^2) \tag{2}$$

where $\tau_o = \frac{2R}{c}$ is the two-way return delay for a target at a distance *R*.

The transmitted and received signals are then mixed together and low pass filtered to obtain the beat frequency signal corresponding to the delay τ_o as

$$S_b(t) = \cos 2\pi (f_o \tau_o + \alpha t \tau_o - \frac{1}{2}\alpha {\tau_o}^2) \tag{3}$$

First term in (3) is a constant phase, the second term $\alpha t \tau_o$ represents the beat frequency which is a measure of therange to

target and is resolved in the frequency domain by performing an FFT. The last term is called residual video phase error and can be compensated.

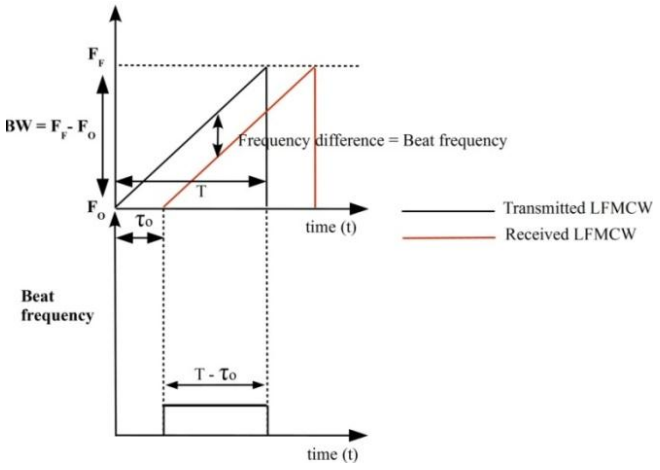

Figure 1 Principle of beat frequency generation in FM-CW operation

III. DDS-Based L-Band FM-CW Hardware Design and Simulation

The complete hardware schematic of low power L-band FM-CW radar using commercial off-the-shelf electronic components is shown in **Figure 2**. A linear FM sweep from 150 MHz to 256 MHz with a very low phase noise output is generated using AD 9858-based Direct Digital Synthesizer (DDS) board. The DDS is programmed using a microcontroller which also controls the start/stop time and the bandwidth for generating a linear saw-tooth FM sweep. The FM chirp sweep bandwidth is up-converted to 1.45-1.55 GHz using an integrated programmable PLL/VCO-based mixer (RFMD-2052) which provides a stable output carrier frequency with low phase noise. The up-converted FM sweep is band limited using a band pass filter of 100 MHz bandwidth realized using micro-strip transmission line. The up-converted FM sweep signal is time delayed using transmission line -based delay line. The delayed signal is mixed with its non-delayed counterpart in the mixer provided in the AD 9858 DDS board to obtain the beat frequency corresponding to the time delay.

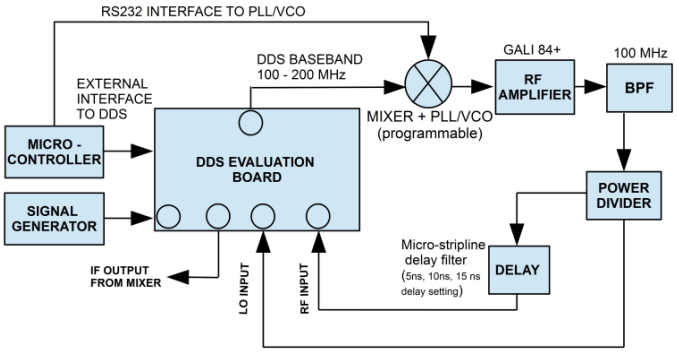

Figure 2 DDS based FM-CW transmitter and receiver design block diagram

In order to understand the behavior of the proposed hardware in **Figure 2**, a design simulation of the subsystem blocks is presented in Matlab®Simulink® environment in **Figure 3**.

The simulation design consists of a baseband FM sweep of 100 MHz bandwidth and sweep time of 40 μs. A PLL block as shown in **Figure 3** with a detailed explanation in **Figure 6** is modeled for a stable carrier frequency of 1.5 GHz. The baseband FM sweep is up-converted to the PLL output frequency using a multiplier block. A band-pass filter with pass band frequency of 1.5-1.6 GHz selects the upper side band of the up-converted sweep spectrum. The up-converted single sided sweep spectrum is multiplied with a delayed copy of itself to produce a beat signal corresponding to backscatter delay from a range of 2.25 m. A delay of 10 ns is modeled using the delay block. To obtain the beat signal, output of multiplier is passed through a low pass filter of cut off frequency 100 KHz.

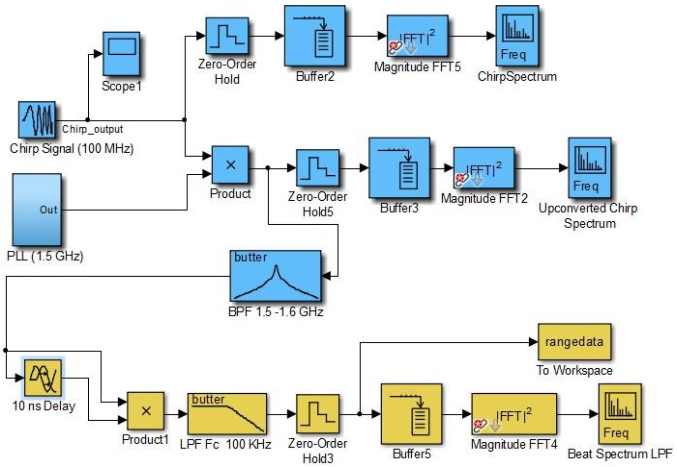

Figure 3 DDS-based FM-CW transmitter and receiver design model simulated in Matlab®Simulink®

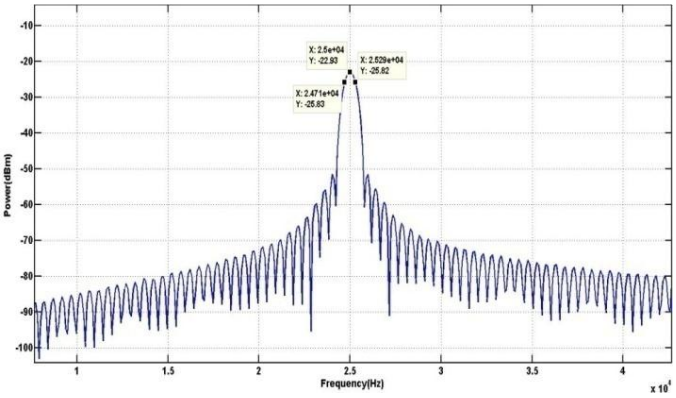

Figure 4 Beat frequency spectrum simulated in Matlab®Simulink®

For observing the frequency spectrum, output of each block is sampled at Nyquist rate using a zero order hold. The sampled signal is buffered using a 2048-point buffer block, and an FFT of same size is performed. The calculated beat frequency is

$$f_b = \alpha\tau = \frac{BW}{T}\cdot\tau = \frac{100e^6}{40\ \mu s}\cdot(10\ ns) = 25\ kHz \quad (4)$$

The obtained beat frequency from the simulation result is 25 KHz as shown in **Figure 4**. This is in agreement with the theoretically calculated value in (4).

A simulink model of PLL is presented in sub-section IV.A with detailed explanation of the individual blocks.

IV. PLL-VCO WITH THIRD ORDER LOOP FILTER DESIGN AND SIMULATION

As described in section IV, the up-conversion mixer consists of an inbuilt PLL/VCO based local oscillator (LO) frequency generator. The inbuilt PLL is a charge pump PLL. The settling time required to attain the stable desired LO frequency is an important parameter in the transmitter design consideration. From the settling time of VCO output, the IF output settling time is calculated for finding the valid beat frequency data period. In this section, we analyze the behavior of the charge pump PLL for its settling time and its effect on the produced beat frequency at the output of the mixer. A PLL is a feedback control circuit that operates by trying to lock to the phase of an input signal by utilizing its negative feedback path [5].A basic form of a PLL consists of three fundamental functional blocks namely phase frequency detector (PD), loop filter (LF), voltage-controlled oscillator (VCO) with the circuit configuration shown in **Figure 5** [6].

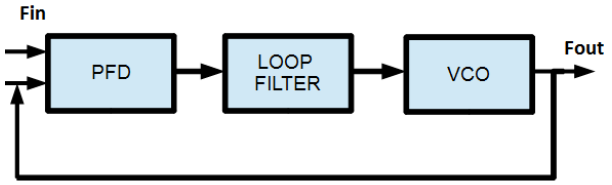

Figure 5 General block diagram of components of PLL

For understanding the behavior of the charge pump PLL along with its individual component blocks, a behavioral model is created in Simulink® as shown in **Figure 6**.

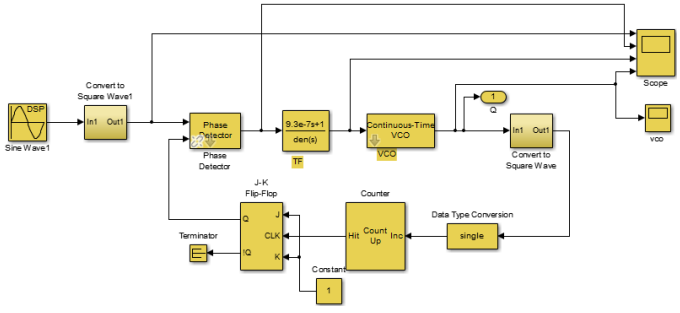

Figure 6 Simulink® model of PLL with third order loop filter

The reference frequency of 4.8MHz (Sine wave1 block) is given as one of the input to Phase detector; the other input which is a feedback signal comes from Continuous-Time VCO output block. The divider is a digital up-counter whose count value is set to 312. The loop filter bandwidth decides the settling time of the PLL. A third order loop filter is designed which has a settling time of 6µs. Specifications of individual blocks of PLL are designed as explained in following subsections.

A. Phase detector and charge pump design

The Phase Detector block consists of two D-type flip flops as shown in **Figure 7**. Output of flip-flop1 enables a positive current source, and that of flip-flop 2 enables a negative current source. The difference in phase between the reference (Sine Wave1 output) and feedback signal (Continuous Time VCO output) is measured by the Phase detector. If there is a phase difference between the two input signals, it generates up or down-synchronized signals to the charge pump and low pass filter as shown in **Figure 8**.

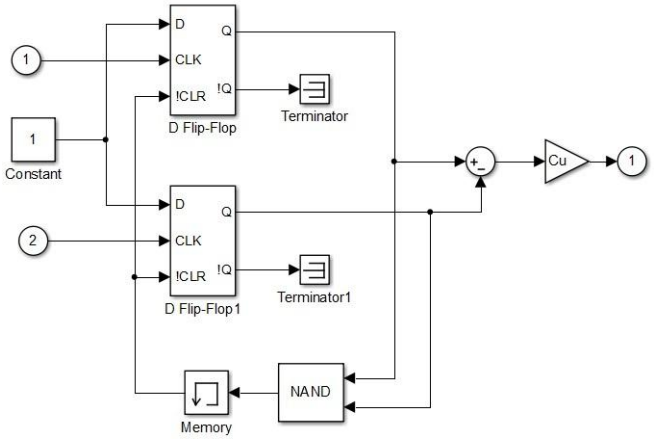

Figure 7 Phase Detector block consisting of two D-flip flops

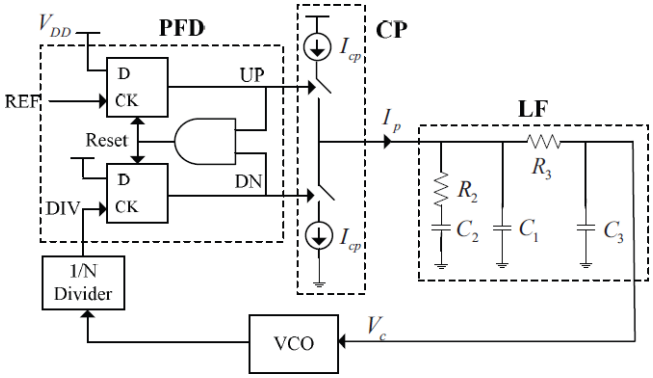

Figure 8 Phase Detector along with charge pump (CP) and loop filter (LF)

The output of Phase Detector (shown as PFD) goes to a charge pump circuit (shown as CP) as shown in **Figure 8** which converts the digital output of PFD into an analog signal. Working of charge pump is shown in **Figure 8**. The charge pump consists of a current source, a current sink and two switches. The charge pump is usually followed by a passive loop filter (LF) that integrates the charge pump output current to a VCO control voltage. The charge pump either sources or sinks current according to the UP and DN signal. This current is converted into a control voltage by the loop filter for tuning the

VCO. The control voltage increases when the reference signal leads the feedback signal and vice-versa.

If I_{cp} is the average source and sink current of the charge pump, the phase detector gain is given by [7]

$$K_d = \frac{I_{\text{cp}}}{2\Pi} \tag{5}$$

where, K_d is the phase detector gain.

B. Loop filter design

The loop filter in the PLL chain sets the settling time of the VCO output [13]. A third order loop filter for the PLL is simulated using Simulink® and ADIsimPLL®[8]software for studying the response of the PLL using the design parameters [9].

The design calculations for finding the loop filter coefficients for a passive two pole loop filter along with a single-pole spur filter (formed by R2 and C3) are based upon **Figure 9**. The PLL output natural frequency is given by

$$\begin{aligned} f_n &= \frac{-1}{2\Pi \cdot t_s \cdot \eta} \cdot \ln\left(\frac{f_a}{f_{step}}\right) \\ &= \frac{-1}{2\Pi \cdot 500\ \text{ns} \cdot 0.707} \cdot \ln\left(\frac{920\ \text{MHz}}{100\ \text{MHz}}\right) \\ &= 1.04\ \text{MHz} \end{aligned} \tag{6}$$

f_{step} Maximum frequency change during a step from one frequency to another

f_a Frequency step after locking of PLL

η Damping factor,where0.707 is the typical choice for 45° phase margin

t_s Desired time for the carrier to step to a new frequency

I_{cp} Charge Pump average Current is taken as 1 mA

K_{vco} sensitivity of VCO

The PLL–VCO divider is the ratio of output L-band frequency to the reference frequency at input of PLL and calculated as

$$N = \frac{1.5GHz}{4.8\text{MHz}} = 312 \tag{7}$$

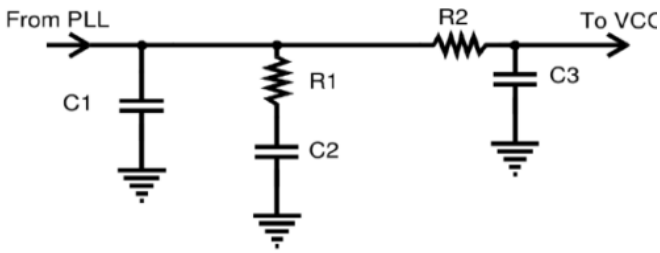

Figure 9 Third order loop filter

The loop filter coefficients are calculated using following formulae

$$\begin{aligned} C2 &= \frac{I_{\text{cp}} \cdot K_{vco}}{\text{N} \cdot (2\Pi \cdot f_n)^2} \\ &= \frac{1\ \text{mA} \cdot 30\ \text{MHz}}{312 \cdot (2\Pi \cdot f_n)^2} = 92\ \text{pF} \end{aligned} \tag{8}$$

$$R1 = 2 \cdot \eta \cdot \sqrt{\frac{N}{I_{\text{cp}} \cdot K_{vco} \cdot C2}} = 15\ \text{K} \tag{9}$$

$$C1 = \frac{\text{C2}}{10} = 9.2\ \text{pF} \tag{10}$$

$R2$ and $C3$ are used to reduce the spurs caused by the reference frequency and their product should be at least one tenth the product of $R1$ and $C2$.

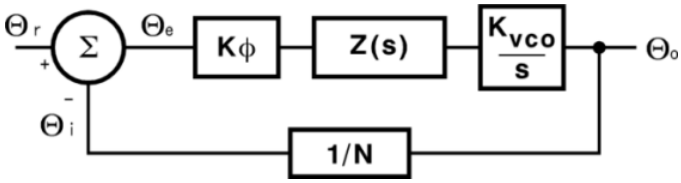

Figure 10 Phase-domain model of the charge pump-PLL

A phase-domain model [9] for the charge pump-PLL is shown in **Figure 10**, where Θ_r is the phase of the reference clock, Θ_i is the phase of the divider output signal, Θ_e is the phase of the error signal, K_{vco} is the VCO gain, T_d is loop delay, and *N* is the division ratio.

The transfer function of the loop filter *Z*(*s*) [11] is given by

$$Z(s) = \frac{sR_2C_2 + 1}{\beta_3 s^3 + \beta_2 s^2 + \beta s} \tag{11}$$

where

$$\beta = C_1 + C_2 + C_3 \tag{12}$$

$$\beta = R_2C_2(C_1 + C_3) + R_3C_3(C_1 + C_2) \tag{13}$$

$$\beta = R_2R_3C_2C_3 \tag{14}$$

Using the above equations the filter coefficients are obtained. The simulation result of the output of charge pump PLL is shown in **Figure 11**. From the simulation result of **Figure 11(b)** a settling time of 6 µs is observed.

C. Voltage controlled oscillator design

The output frequency of VCO depends on the controlled voltage V_{ctrl} [12] such that

$$F_{ctrl} = F_o + K_{vco} + V_{ctrl} \tag{15}$$

The output phase of the VCO is calculated as

$$\Phi_{VCO}(t) = \Phi_O + 2\Pi \cdot K_{vco} \cdot \int V_{ctrl}(t) \cdot dt \tag{16}$$

where, F_o is the free running frequency at $V_{ctrl} = 0$, Φ_O is the initial output phase of the VCO.

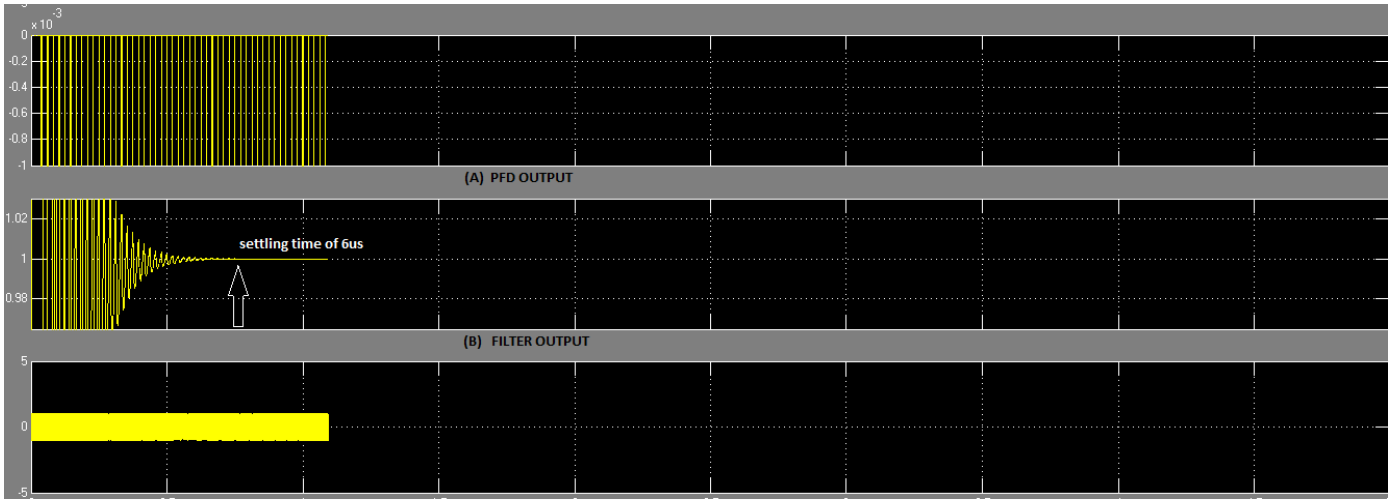

Figure 11 Simulation results of PLL using 3rd order loop filter.
(a) Phase Detector output; (b) Loop filter output showing the settling time; (c) The RF output of VCO

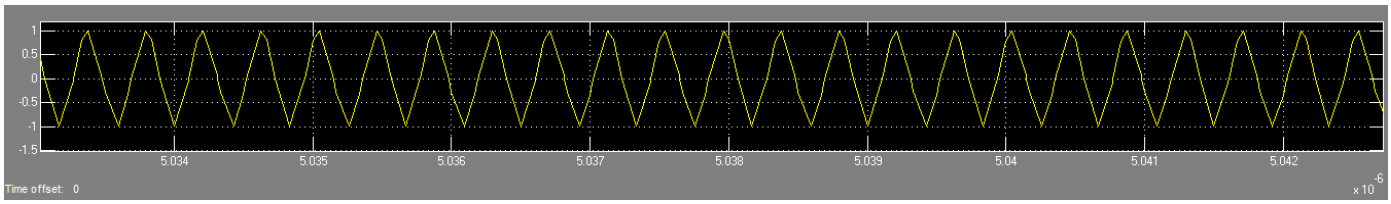

Figure 12 VCO simulation output at 1.5GHz at locking position

Laplace transform of VCO transfer function is given as

$$\frac{\Phi_{VCO}(t)}{V_{ctrl}(t)} = 2\Pi \frac{Kvco}{s} \tag{17}$$

The VCO sensitivity or gain is calculated by

$$K_{vco} = \frac{F_{\max} - F_{\min}}{V_{\max} - V_{\min}} = \frac{(1.5 - 1.35)\ \text{GHz}}{(5-0)\text{V}} = 30\ \text{MHz/V} \tag{18}$$

where $F_{\max}$ and $F_{\min}$ are the maximum and minimum VCO output frequencies respectively. $V_{\max}$ and $V_{\min}$ are the maximum and minimum VCO input voltages respectively.

An L-band radar altimeter hardware is developed according to the parameters of the simulations described in Section IV and V. The hardware realization along with measured test results is described in the following section.

V. Hardware Implementation at L-Band

The complete hardware is designed and fabricated according to the block diagram shown in **Figure 2**. The measurement setup for testing the hardware is shown below in **Figure 13**. The aluminum chassis consists of a PIC 124 FJ microcontroller board, RFMD 2052 mixer/PLL-VCO IC, GALI-84+ microwave amplifiers and transmission line filter. The 100 MHz sweep is generated from DDS (AD9858) evaluation board. The reference frequency of 1GHz that provides a clock frequency to AD9858 DDS evaluation board is generated using Rohde& Schwarz signal generator.

FM sweep spectrum of 100 MHz bandwidth and a signal power of -7.8 dBm is obtained at the DDS output as shown in **Figure 14**.

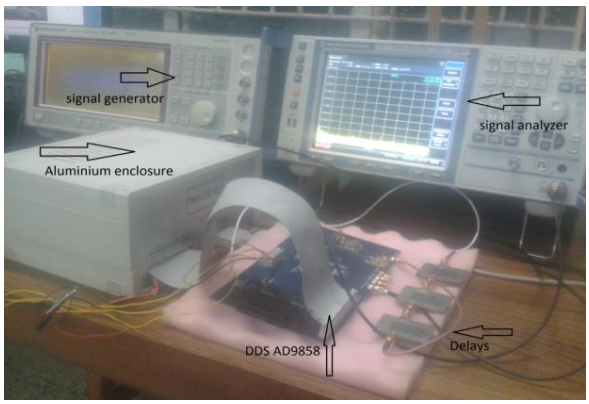

Figure 13 Laboratory hardware setup for FM-CW altimeter trans-receiver

The output of the DDS with high spectral purity and low phase noise can be seen in **Figure 15**. The phase noise of the DDS output frequency is measured to be -94.67 dBm at 10 kHz offset. The mixer has an inbuilt integrated PLL-VCO for LO generation. The LO frequency of 1.5 GHz generated in the mixer is shown in **Figure 16**.The RFMD-2052 is a wideband RF frequency converter chip which includes a fractional-N phase-locked loop, a crystal oscillator circuit, a low noise VCO

core, an LO buffer, and an RF mixer. The up-converted FM sweep shown in **Figure 17** has a nonlinear power spectrum. The integrated PLL-VCO in the mixer is driven by an uncompensated reference frequency source due to which the nonlinear behavior is observed.

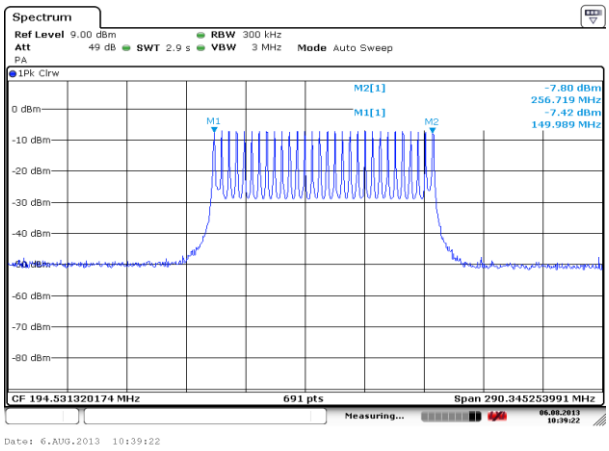

Figure 14 FM sweep bandwidth of 100 MHz generated using DDS

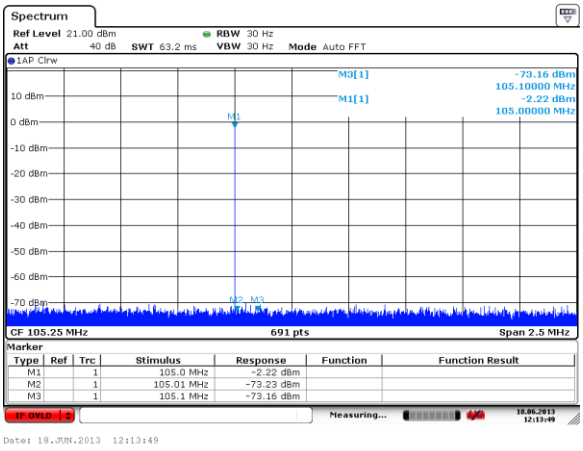

Figure 15 Phase noise measurement for sine wave at 105 MHz of DDS output

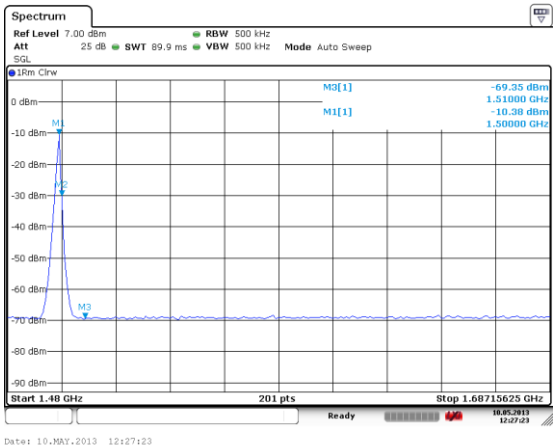

Figure 16 LO frequency of mixer at 1.5 GHz

The beat frequency measurement results for the L-band radar hardware have not been shown in the paper. Meanwhile an X-band FMCW radar hardware has been developed by the collaborators [14]. Measured results for the calibration of the X-band radar hardware are presented in section VI to show the efficacy of FMCW radar altimeter for range measurement. Similar test results will be obtained for L-band radar hardware.

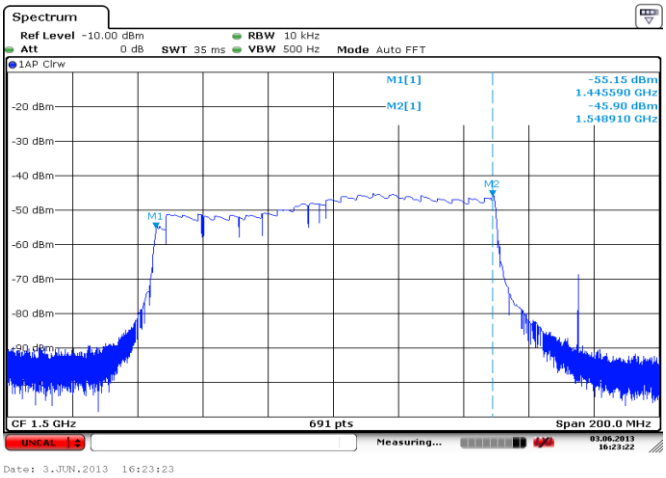

Figure 17 Upper sideband of up-converted chirp spectrum at mixer output

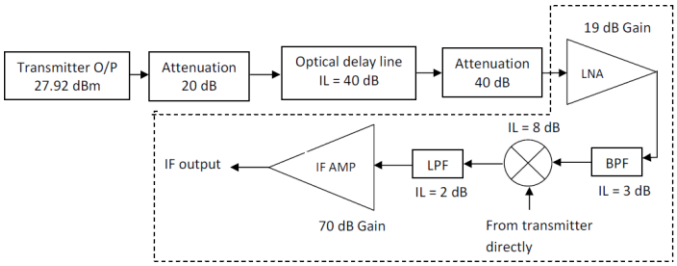

Figure 18 X-band hardware in loop test setup block diagram

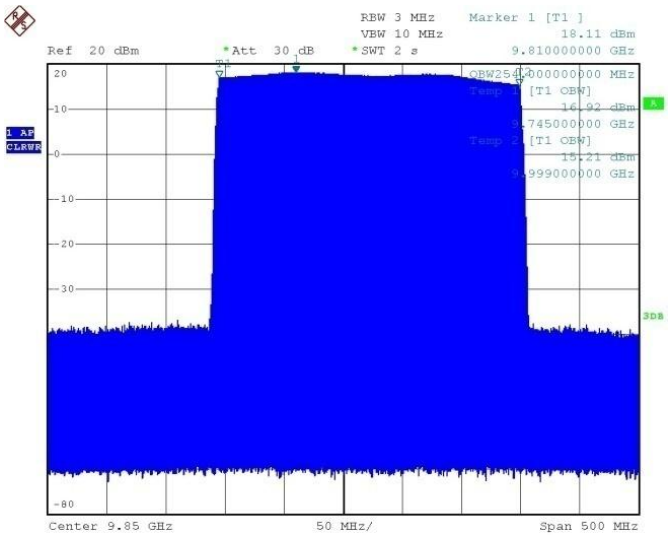

Figure 19 Generated FM sweep of 254 MHz at transmitter output

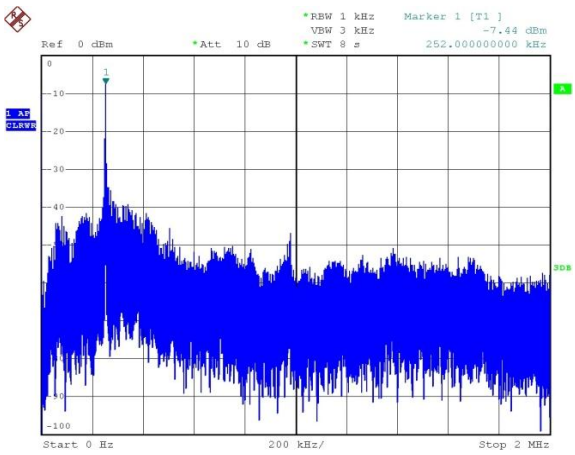

Figure 20 Measured beat frequency of 252 KHz at IF output

VI. Test Results for X-Band Radar

The hardware-in-loop setup for calibrating the X-band transmitter-receiver for beat frequency measurement at the IF output is shown in **Figure 18**. An FM sweep of 2 ms duration and 254 MHz bandwidth at a carrier frequency of 9.7 GHz with transmitted power of 27.92 dBm is shown in **Figure 19**. The transmitter output is routed to the receiver through an optical loom which simulates the two-way backscatter delay. The measured beat frequency of 252 KHz at the IF output directly using a spectrum analyzer corresponding to a loom delay setting of 300 m is shown in **Figure 20**.

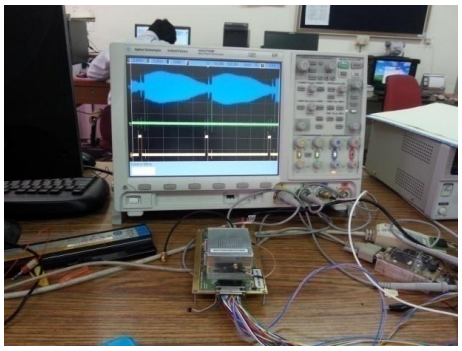

Figure 21 Test setup for digitized IF output measurement on digital storage oscilloscope

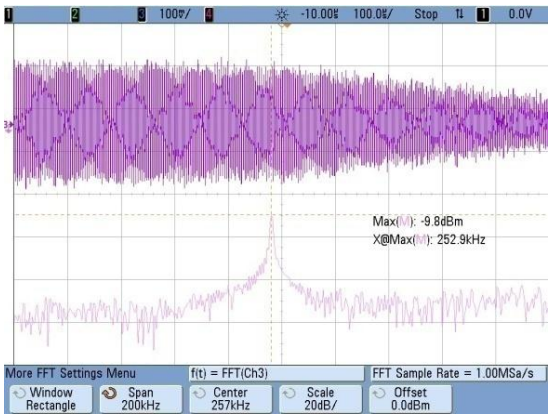

Figure 22 Time and frequency domain display of digitized IF output data

The digitized IF output is measured using a digital storage oscilloscope (DSO) as shown in the laboratory setup in **Figure 21**. The time domain beat data corresponding to subsequent sweeps of 2 ms is seen on the DSO An enlarged view of the time domain beat data along with its frequency spectrum is shown in **Figure 22**. From the comparison of **Figure 20** and **Figure 22** it is seen that the measured IF output beat frequency values are nearly the same before and after digitization.

VII. Concluding Remarks

We have shown in this paper laboratory demonstration of a DDS-based FM-CW transmit-receive system with a transmission line-based delay to measure the specification of an L-band radar altimeter. It is observed that for a 100 MHz sweep bandwidth using DDS, the phase noise is considerably low. Moreover, we have shown the detailed design of a third order loop filter for the PLL–VCO combination with a low settling time. Measured results for the calibration of an X-band FMCW radar hardware are also presented to demonstrate the feasibility of FMCW radar altimeter.

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